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328654(28)

B.E. (Sixth Semester) Examination April-May 2020

(New Scheme)

(Et & T Branch)

VLSI DESIGN

Time Allowed : Three hours

Maximum Marks : 80

Minimum Pass Marks : 28

Note : *Attempt all questions. Part (a) of each question is compulsory, which is of 2 marks. Attempt any* ***two*** *parts from (b), (c) and (d) each is of 7 marks.*

Unit-I

1. (a) What is Moore's law? Explain. 2

(b) Explain front end design and back end design using VLSI design flow. 7

(c) What is CMOS transmission gate? Design XOR Gate using CMOS transmission gate. 7

(d) Design the following logics using CMOS :

(i) $AB + \overline{B}C + (A + B) \cdot C$ 4

(ii) $AB + \overline{A}\overline{B}$ 3

Unit-II

2. (a) What is Euler Graph? 2

(b) Draw and explain fabrication process of nMOS with suitable diagram. 7

(c) What do you mean by Lambda based design rule? Discuss in detail with suitable diagram. 7

(d) Draw the schematic, stick diagram and layout for 2-input CMOS NAND Gate. 7

Unit-III

3. (a) What is W/L Ratio? 2

(b) Construct stick diagram and layout of Half Adder. 7

(c) What are semi conductor memories? Explain SRAM & DRAM in detail. 7

(d) Draw the schematic diagram and layout of $1 - T$ DRAM cell. 7

Unit-IV

4. (a) What do you understand by SSI, MSI, LSI, VLSI and ULSI? 2

(b) Explain If / Else statement with their syntax in VHDL and write VHDL code for full adder using If / Else statement. 7

(c) Write the VHDL code for 4-bit Adder using structural modeling style. 7

(d) Write the syntax of the following in VHDL : 7

(i) Library Declaration

(ii) Entity Declaration

(iii) Architecture Declaration

(iv) Case Statement

Unit-V

5. (a) Write the two difference between Mealy and Moore FSM. 2

(b) Write the VHDL code for JK Flip-flop. 7

(c) Design a 4-bit up counter using VHDL and write their code. 7

(d) What do you understand by test bench? Write a test bench for full adder in VHDL. 7